What is claimed is:

1. A method of manufacturing a ferroelectric memory device, comprising steps of:

(a) forming a peripheral circuit section for selectively writing information into or reading information from the memory cell over a semiconductor substrate; and

(b) forming at least first signal electrodes, second signal electrodes arranged in a direction intersecting the first signal electrodes, and a ferroelectric layer disposed at least in intersection regions between the first signal electrodes and the second signal electrodes, and forming a memory cell array in which memory cells are arranged in a matrix,

wherein the peripheral circuit section is formed in a region outside the memory cell array.

2. The method of manufacturing a ferroelectric memory device according to claim 1,

wherein the step (b) comprises steps of:

(b-1) forming the first signal electrodes;

(b-2) forming the ferroelectric layer; and

(b-3) forming the second signal electrodes.

3. The method of manufacturing a ferroelectric memory device according to claim 2,

wherein the step (b-2) comprises a step of forming an amorphous ferroelectric layer or a microcrystalline ferroelectric layer, and a step of forming the ferroelectric layer by subjecting the amorphous ferroelectric layer or the microcrystalline ferroelectric layer to a heat treatment.

4. The method of manufacturing a ferroelectric memory device according to claim 2,

wherein the step (b-2) is a step of forming the ferroelectric layer linearly along the first signal electrodes.

5. The method of manufacturing a ferroelectric memory device according to claim 4, further comprising:

a step of forming, over a base, a first region having a surface characteristic which causes a material for forming at least one of the first signal electrodes or the ferroelectric layer to be deposited preferentially, and a second region having a surface characteristic which causes a material for forming at least one of the first signal electrodes or the ferroelectric layer to be less deposited than the first region; and

a step of providing a material for forming at least one of the first signal electrodes or the ferroelectric layer and selectively forming the material in the first region.

6. The method of manufacturing a ferroelectric memory device according to claim 5,

wherein the first region and the second region are formed on a surface of the base.

7. The method of manufacturing a ferroelectric memory device according to claim 6,

wherein a surface of the base is exposed in the first region, and

wherein a surface-modifying layer that has a surface characteristic exhibiting weaker affinity to the material for forming the first signal electrodes and the ferroelectric layer

than the exposed surface of the base in the first region is formed in the second region.

8. The method of manufacturing a ferroelectric memory device according to claim 6,

wherein a surface of the base is exposed in the second region, and

wherein a surface-modifying layer that has a surface characteristic exhibiting stronger affinity to the material for forming the first signal electrodes and the ferroelectric layer than the exposed surface of the base in the second region is formed in the first region.

9. The method of manufacturing a ferroelectric memory device according to claim 4,

wherein a dielectric layer is provided between laminates formed of the first signal electrodes and the ferroelectric layer so as to cover exposed areas of the base.

10. The method of manufacturing a ferroelectric memory device according to claim 9,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

11. The method of manufacturing a ferroelectric memory device according to claim 2,

wherein the ferroelectric layer and the second signal electrodes are formed in a direction intersecting the first signal electrodes, and

wherein the ferroelectric layer is formed linearly along

the second signal electrodes.

12. The method of manufacturing a ferroelectric memory device according to claim 11,

wherein the ferroelectric layer and the second signal electrodes are patterned by etching using the same mask.

13. The method of manufacturing a ferroelectric memory device according to claim 11,

wherein a dielectric layer is provided between laminates formed of the ferroelectric layer and the second signal electrode so as to cover exposed areas of the base and the first signal electrodes.

14. The method of manufacturing a ferroelectric memory device according to claim 13,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

15. The method of manufacturing a ferroelectric memory device according to claim 2, further comprising:

a step (b-4) of patterning the ferroelectric layer after the step (b-3), and causing the ferroelectric layer to remain in a shape of a block only in intersecting regions between the first signal electrodes and the second signal electrodes.

16. The method of manufacturing a ferroelectric memory device according to claim 15, further comprising:

a step of forming, over the base, a first region having a surface characteristic which causes a material for forming at least one of the first signal electrodes or the ferroelectric

layer to be deposited preferentially, and a second region having a surface characteristic which causes a material for forming at least one of the first signal electrodes or the ferroelectric layer to be less deposited than the first region; and

a step of providing a material for forming at least one of the first signal electrodes or the ferroelectric layer and selectively forming the material in the first region.

17. The method of manufacturing a ferroelectric memory device according to claim 16,

wherein the first region and the second region are formed on a surface of the base.

18. The method of manufacturing a ferroelectric memory device according to claim 17,

wherein a surface of the base is exposed in the first region, and

wherein a surface-modifying layer that has a surface characteristic exhibiting weaker affinity to the material for forming the first signal electrodes and the ferroelectric layer than the exposed surface of the base in the first region is formed in the second region.

19. The method of manufacturing a ferroelectric memory device according to claim 17,

wherein a surface of the base is exposed in the second region, and

wherein a surface-modifying layer that has a surface characteristic exhibiting stronger affinity to the material for forming the first signal electrodes and the ferroelectric layer

than the exposed surface of the base in the second region is formed in the first region.

20. The method of manufacturing a ferroelectric memory device according to claim 15,

wherein the ferroelectric layer and the second signal electrodes are patterned by etching using the same mask.

21. The method of manufacturing a ferroelectric memory device according to claim 15,

wherein a dielectric layer is provided between laminates formed of the first signal electrodes and the ferroelectric layer so as to cover exposed areas of the base.

22. The method of manufacturing a ferroelectric memory device according to claim 21,

wherein a dielectric layer is provided between laminates formed of the ferroelectric layer and the second signal electrode so as to cover exposed areas of the base and the first signal electrodes.

23. The method of manufacturing a ferroelectric memory device according to claim 21,

wherein the dielectric layer is formed of a material having a dielectric constant lower than a dielectric constant of the ferroelectric layer.

24. The method of manufacturing a ferroelectric memory device according to claim 1, further comprising:

a step (b-5) of forming insulation layers between the first signal electrodes after the step (b-1),

wherein upper surfaces of the insulation layers are on

the same level as upper surfaces of the first signal electrodes.

25. The method of manufacturing a ferroelectric memory device according to claim 24,

wherein the step (b-5) is a step of forming the insulation layers using a solution application process and planarizing the insulation layers.

26. An embedded device comprising:

the ferroelectric memory device as defined in claim 1; and

at least one component selected from a group including a flash memory, a processor, an analog circuit, and an SRAM.